F1: Non-Volatile Memory Circuit Design and Technology

Organizer/Chair: **Mark Bauer,** *Intel, Folsom, CA*

Committee: **Giulio Casagrande,** *ST Microelectronics, Milano,Italy*
Hideto Hidaka, *Renesas, Itami, Hyogo, Japan*
Yair Sofer, *Saifun Semiconductors, Netanya, Isreal*

Solid-state non-volatile memories have seen explosive growth in the last few years in electronic applications such as memory cards, cell phones, still and video cameras, digital music, video players and other consumer electronic devices. With the memory cost per bit reducing at very aggressive rates, the industry is seeing even more solid-state non-volatile memory applications emerging such as disk caches and solid-state disks for use in personal and portable computers. Application requirements for low-cost, low-power, high-performance non-volatile memory, and major challenges associated with aggressively scaling process technologies have driven the industry to many new circuit design, architecture and technology innovations.

Floating gate structures continue to dominate non-volatile memory technology. These structures typically use a polysilicon floating gate as the storage node and are arranged in various memory arrays to achieve architectures such as NAND flash and NOR flash memory. To program and erase the memory cell, electron tunneling methods are used to place or remove electrons from the floating gate. Other material types are being developed as floating gate replacements such as NROM memories where the storage material is a nitride material. Non-electron storage non-volatile memory types such as PRAM (phase-change RAM) and MEMS-based memories are also being researched. Alternative cell structures such as FeRAM (ferro-electric RAM) and MRAM (magnetic RAM) have recently become commercially available. These newer memory types have the potential to be used in existing non-volatile memory sockets or drive new applications.

Many circuit design and architectural innovations have been developed over the years to overcome scaling challenges and improve performance on established non-volatile memory technologies. New circuit and architecture development are required to design a memory using the new cell types and structures. Multi-level design, multi-bit design and, on-chip read/write buffer architectures are just a few examples.

The Advanced Circuits Forum on Non-Volatile Memory Circuit Design and Technology will first present an overview of floating-gate type non-volatile memory cells and structures along with recent advancements in extensions of electron storage with new material types. In addition, new memory cell types and structures using different materials will be discussed along with the challenges associated with integration of new materials into a CMOS technology. The discussion of technology will lay the foundation for the subsequent discussions on design techniques for the various non-volatile memory types. Following the design discussions, we will explore different non-volatile memory applications and how the various memory technologies and designs fit within the range of applications.

This all day forum encourages open exchange in a closed forum. Attendance is limited and pre-registration is required. Coffee breaks and lunch will be provided to allow a chance for participants to discuss the issues and ask follow-up questions to the forum presenters.

Forum Agenda

Time	Topic
8:00	Continental Breakfast
8:30	**Introduction and Overview** **Mark Bauer**, *Intel, Folsom, CA*
9:00	**Non-Volatile Memory Technology: Present and Future Trends** **Al Fazio**, *Intel, Santa Clara, CA*
10:15	Break
10:30	**NOR Flash Memory Design** **Kerry Tedrow**, *Intel, Folsom, CA*
11:30	**NAND Flash Memory Design** **Tomoharu Tanaka**, *Micron, Kamata, Japan*
12:30	Lunch
1:15	**NROM Memory Design** **Yair Sofer**, *Saifun Semiconductors, Netanya, Israel*
2:00	**Embedded Flash Memory Design** **Hideto Hidaka**, *Renesas, Itami, Japan*
2:45	Break
3:00	**Circuits and Design Challenges for Alternative and Emerging NVM** **Shine Chung**, *TSMC, Hsinchu, Taiwan*
4:00	**Non-Volatile Memory Applications** **Koji Sakui**, *Sony, Japan*
5:00	Parting Remarks and Wrap-up

F2: Design of 3D-Chipstacks

Organizer: **Werner Weber**, *Infineon Technologies, Munich, Germany*
Co-Organizer: **William Bowhill**, *Intel, Hudson, MA*

Committee: **Kerry Bernstein**, *IBM Yorktown Heights, NY*
Anantha Chandrakasan, *MIT, Cambridge, MA*
Ronald Ho, *Sun Microsystems, Menlo Park, CA*
Peter Kogge, *University of Notre Dame, Notre Dame, IN*
Samuel Naffziger, *Advanced Micro Devices, Fort Collins, CO*
Hiroyuki Mizuno, *Hitachi, Tokyo, Japan*

Many experts claim that 'Moore's Law' will gradually come to its end and will be replaced by new innovations headlined by the term 'More Than Moore.' Among others, this term comprises advanced multi-chip integration methods such as 3D System Integration. This technology provides high-potential performance benefits in terms of geometry and speed and has drawn major attention by a large number of research groups in the past few years. Numerous process architectures have been developed and the first cost-effective commercialized applications in the communications and memory fields are expected to come to market soon. The objective of this forum is to introduce the different process architectures and present potential applications to be deployed in the coming years.

The forum will provide an overview of the field and the different technological approaches. Digging deeper, it will provide an understanding of potential memory and processor applications giving performance and cost arguments. The forum is intended for circuit and system designers and engineering students wishing to gain insight into this interface between circuit design, system design and packaging and how it may impact applications in the near future.

The forum will start with a technology overview by **Harry Hedler** (Qimonda) highlighting the different process architectures and their benefits and shortcomings. In the second presentation, **Mitsumasa Koyanagi** (Tohoku U) will present prototypes based on wafer-to-wafer stacking and chip-to-wafer stacking. He became a father of 3D integration when he introduced wafer stacking 25 years ago. **Muhannad Bakir** (Georgia Tech) will then address the important topics of heat removal and power distribution in the chip-stacks. The technology section is then concluded with a presentation by **Tadahiro Kuroda** (Keio U) who will address chip-to-chip data communication by inductive and capacitive coupling. The applications section starts with a presentation by **Dan Radack** (DARPA) who provides an overview of possible applications and their advantages and disadvantages. **Wilfried Haensch** (IBM) will then discuss the processor applications, elaborating on alternative integration strategies. **Bryan Black** (Intel) will continue the discussion of processor applications and discuss design challenges of 3D integration. **Dong-Ho Lee** (Samsung) will contrast this with memory applications. The presentation by **Bert Gyselinckx** (IMEC) will highlight the opportunities of 3D integration for miniaturized wireless sensor networks. Finally, **Hannu Tenhunen** (KTH Sweden) will elaborate on the cost and performance trade-offs for 3D mixed signal systems. The forum concludes with a panel discussion, which will provide the audience the chance to engage in extended discussions with the presenters.

Forum Agenda

Time	Topic
8:00	Breakfast
8:20	**Introduction** **Werner Weber**, *Infineon, Munich, Germany*
	3D Technologies
8:30	**Status, Opportunities and Trends of 3D Integration by Thru-Silicon-Via Stacking** **Harry Hedler**, *Qimonda, Munich, Germany*
9:15	**New Three-Dimensional Integration Technologies Based on Wafer-to-Wafer and Chip-to-Wafer Bonding Methods** **Mitsumasa Koyanagi**, *Tohoku University, Sendai, Japan*
10:00	Break
10:15	**Heat Removal and Power Delivery for 3D SoC** **Muhannad Bakir**, *Georgia Institute of Technology, Atlanta*, GA
10:45	**CMOS Proximity Wireless Communications of SiP Integration** **Tadahiro Kuroda**, *Keio University, Yokohama, Japan*
	3D Applications
11:15	**Applications of 3D Integration** **Dan Radack**, *DARPA, Arlington, VA*
11:45	**Is 3D the Next Big Thing in Microprocessors?** **Wilfried Haensch**, *IBM, Yorktown Heights, NY*
12:15	Lunch
1:15	**3D Design Opportunities and Challenges for Microprocessors** **Bryan Black**, *Intel, Austin, TX*
1:45	**3D Chip Stacking Technology for Memory Device** **Dong-Ho Lee**, *Samsung, Yongin City, Korea*
2:30	Break
2:45	**3D System-in-Package Integration of Wireless Sensor Nodes** **Bert Gyselinckx**, *IMEC, Leuven, Belgium*
3:30	**Performance and Cost Trade-Offs for SoC, SoP and 3D Integration** **Hannu Tenhunen**, *Royal Institute of Technology, Kista, Sweden*
4:00	Panel discussion
5:00	Conclusion

F3: Power Amplifiers and Transmitter Architectures

Organizer: **Rudolf Koch,** *Infineon Technologies, Germany*
Co-Organizer: **Francesco Svelto**, *University of Pavia, Pavia, Italy*

Committee: **David Su,** *Atheros Communications, Santa Clara, CA*
Tony Montalvo, *Analog Devices, Raleigh, NC*
Ali Hajimiri, *California Institute of Technology, Pasadena, CA*
Aarno Paerssinen, *Nokia, Helsinki, Finland*
Arya Behzad, *Broadcom, San Diego, CA*

In this all-day forum, new trends in power amplifiers and (PAs) transmit architectures for wireless communications will be discussed.

Mobile phones are evolving from single-standard voice phones to multi-standard multi-band multi-application mobile terminals. High integration levels and re-configurability of the signal processing chain are a must for those all-in-one phones to minimize chip area and cost, but have so far only been demonstrated in transceivers. For entry-level phones single-chip transceiver and baseband integration is a reality now. Power amplifiers, however, have so far been resisting this trend — at least in cellular applications. One PA per band and per standard will be too bulky and too expensive for future terminals. Future PAs must be reconfigurable to support several standards. Silicon integration is a requirement for "intelligent" PAs and is promising cost reduction over III-V PAs, but can it handle the power levels and peak voltages of cellular phones? A variety of PA architectures promises high PAE under certain conditions. For power efficient structures it is, however, no longer sufficient to optimize the PA alone. Rather co-development and common optimization of transmitter, PA, and power supply is required. This forum will highlight the latest trends in PA and transmitter design.

The morning session begins with an introduction into the topic by **David Su** (Atheros). The second speaker, **Earl McCune** (Panasonic) will discuss transmit architectures, their impact on the PA concept, and show practical results for various approaches. The third and last speaker of the morning session, **David Pehlke** (Silicon Labs) will look in detail into a variety of PA concepts and linearization techniques and explain their tradeoffs.

The afternoon session will be opened by **Lawrence Larson** (UC San Diego), who will show how the various power supply modulation schemes can be used to enhance PA efficiency. Special attention will be given to OFDM applications. The fifth speaker, **Gene Tkachenko** (Skyworks Solutions) will cover technology requirements and solutions for cellular PAs and front-end modules. The effects of critical system parameters on technology choice will be explained. Finally, **Ali Hajimiri** (CalTech) will show novel circuit concepts enabling CMOS integration of power amplifiers even for GSM.

The forum will conclude with a panel discussion, where the attendees have the opportunity to ask questions and to share their views.

Attendance is limited and pre-registration is required. This all-day forum encourages open information exchange.

The targeted participants are circuit designers and concept engineers working on wireless transmitters or power amplifiers who want to learn about the latest developments in system and circuit design.

Forum Agenda

Time	Topics
08:00	Breakfast
08:30	**Welcome** **Rudolf Koch,** *Infineon, Munich, Germany*
08:45	**Introduction and Basics** **David Su,** *Atheros Communications, Santa Clara, CA*
09:15	**Transmit Architectures and Power Amplifier Requirements** **Earl McCune,** *Panasonic, Santa Clara, CA*
10:45	Coffee Break
11:15	**Power Amplifier Concepts** **David Pehlke,** *Silicon Labs, Austin, TX*
12:45	Lunch Break
2:15	**Power Supply Modulation Techniques for Power Amplifier Efficiency Enhancement** **Lawrence Larson;** *University of California at San Diego, La Jolla, CA*
3:00	**Overview of Power Amplifier and Front-End Module Technologies and Solutions** **Gene Tkachenko,** *Skyworks Solutions, Woburn, MA*
3:45	Coffee Break
4:15	**Fully Integrated CMOS Power Amplifiers for Mobile WirelessCommunications** **Ali Hajimiri,** *California Institute of Technology, Pasadena, CA*
5:00	Panel Discussion
5:30	Conclusion

F4: Noise in Imaging Systems

Organizer: **Albert Theuwissen,** *DALSA, Eindhoven, Netherlands*

Committee: **Dan McGrath,** *Eastman Kodak, Rochester, NY*
Jed Hurwitz, *Gigle Semiconductor, Edinburgh, United Kingdom*
Hirofumi Sumi, *Sony, Tokyo, Japan*
Boyd Fowler, *Fairchild Imaging, Milpitas, CA*
Makoto Ikeda, *University of Tokyo, Tokyo, Japan*
Takao Kuroda, *Matsushita, Kyoto, Japan*
Johannes Solhusvik, *Micron Technology, Pasadena, CA*
Yonghee Lee, *Samsung, Gyeonggi-Do, Korea*

Noise in Imaging Systems has much in common with noise in the classical world of analog electronics, but imaging adds some very specific noise issues to consider. In many cases the electronic engineer only refers to temporal noise when discussing noise, but in an imaging system non-temporal noise sources also need to be taken into account. In addition, the perfect image sensor in a perfect camera still suffers from noise, because of the photon shot noise of the input signal.

This forum is organized to contribute to a better understanding of noise issues in imaging systems and to stimulate creativity in this field. The speakers at this forum are world experts in this area.

Takao Kuroda (Matsushita) will introduce the topic to begin the forum. The next talk, by **Boyd Fowler** (Fairchild Imaging), will discuss several noise mechanisms starting with the most important one, kT/C noise. The kT/C noise sets a fundamental detection limit on capacitive sensors. Therefore it is important to understand the factors that determine the kT/C noise and how this noise may be mitigated.

Bedrabata Pain (JPL) will speak on the topic of device-level noise. The pixels in imagers are becoming extremely small and several noise sources can be distinguished within every pixel. Shrinking the CMOS technology will put constraints on the pixel's noise behavior.

A CMOS imager is usually a complex mixed analog-digital system-on-chip and circuit noise often dominates the total noise of the image sensor. The circuit noise is observed as a fixed pattern noise or a temporal random noise. The former is originated by device mismatches and is cancelled in the analog and/or digital domains, while the latter is more problematic. **Shoji Kawahito** (Shizuoka U) will discuss noise at the circuit level.

One level higher than the circuit is the system level. Each of the system elements plays an important role in determining the overall noise of the system. The optics may introduce noise in the form of stray signals, such as flare and ghost images, both of which result from internal reflections. A system-level view must also consider factors such as the pixel spectral response, which affects noise amplification, as well as the noise originating from power supply variation, timing jitter, and imperfect FPN cancellation circuits. The speaker invited to talk about system-level noise is **Rick Baer** (Micron Technology).

Random noise and distortion added to an image signal only matters when it can be seen. Seeing it however does not necessarily mean that it will be considered as a defect. Visual artists learn to use the features of a technology that impart a distinctive look to the resulting image for artistic goals. **Jim Larimer** (ImageMetrics) will review the properties of the human visual system that allow viewers to see distortion and noise in the temporal, spatial and intensity domains of the image, how the eye samples the signal and how this process can "beat" with capture and reconstruction methods.

The last presentation of the forum will highlight some algorithms used to cancel noise in images. **Aleksandra Pizurica** (Ghent U) will review some of the latest and best available multiresolution methods for noise reduction. Attention will be given to the following topics: estimation of the noise statistics from the input image (or video); construction of spatially adaptive denoising methods; motion estimation/compensation and noise suppression adapted to motion estimation reliability. In addition, some application specific topics, such as the use of "noise patterns" and camera reference frames for denoising digital camera images will be reviewed.

Although this forum focuses on imaging systems, the issues and techniques dealt with are also applicable to other emerging fields.

Forum Agenda

Time	Topic
8:00	Breakfast
8:30	**Welcome and Overview** **Albert Theuwissen,** *DALSA, Eindhoven, The Netherlands*
8:40	**The 4 Dimensions of Noise** **Takao Kuroda**, *Panasonic, Kyoto, Japan*
9:20	**kT/C noise** **Boyd Fowler**, *Fairchild Imaging, Milpitas, CA*
10:15	Break
10:30	**Noise at the Device Level** **Bedrabata Pain,** *JPL, Pasadena, CA*
11:25	**Noise at the Circuit Level** **Shoji Kawahito,** *Shizuoka University, Hamamatsu, Japan*
12:20	Lunch
1:20	**Noise at the System Level** **Rick Baer,** *Micron Technology, San Jose, CA*
2:15	**Perception of Noise in Imagery** **Jim Larimer**, *ImageMetrics, Half Moon Bay,CA*
3:10	Break
3:25	**Noise Reduction** **Aleksandra Pizurica,** *Ghent University, Ghent, Belgium*
4:20	Panel discussion – All speakers and committee members
4:50	Conclusion

F5: ATAC: Automotive Bus Systems

Organizer/Chair: **Wolfgang Pribyl**, *Graz University of Technology, Austria*
Co-Chair: **Herman Casier**, *AMI Semiconductor, Oudenaarde, Belgium*

Committee:
Franz Dielacher, *Infineon Technologies, Villach, Austria*
Muneo Fukaishi, *NEC, Kanagawa, Japan*
Bob Payne, *Texas Instruments, Dallas, TX*
Bill Redman-White, *NXP, Southampton, United Kingdom*
Doug Smith, *SMSC, Phoenix, AZ*
Sam Naffziger, *AMD, Fort Collins, CO*
Jos Huisken, *Silicon Hive, Eindhoven, The Netherlands*
Atila Alvandpour, *Linköping University, Sweden*

This all-day forum is dedicated to automotive bus systems, giving an overview from the physical layers to the higher levels (processors, protocols) up to the system perspective and implementation issues in a recently introduced car platform.

Electrical and system design issues will be discussed as well as the important field of EMC and other aspects of the harsh automotive environment. Processors and protocols will be presented as well as overall system aspects, which have to be taken into account when choosing the bus systems for a car platform.

This forum will begin with an overview of different bus systems used in automotive applications by **Herman Casier** (AMI Semiconductor). In the next presentation **Martin Peteratzinger** (BMW) will discuss the criteria for bus system selection and optimization, based on the development experience with a recent car platform.

The following two papers focus on physical layer aspects. **Geert Vandensande** (AMI Semiconductor) and **Harald Gall** (austriamicrosystems) will discuss LIN & CAN bus and Flexray, respectively. They will emphasize the bus-characteristics and design considerations to cope with low-cost and harsh automotive environment requirements.

The next talk will concentrate on processors and protocols for bus systems. **Shunichi Ko** (Fujitsu) will use Flexray as an example for the discussion of this topic.

Dave Knapp (SMSC) will focus on the MOST network as a backbone for the multimedia-enabled car in the next presentation. Safety and dependability is the topic of the concluding presentation. From a system perspective, **Stefan Poledna** (TTTech) will in this paper highlight the needs and state-of-the-art of automotive busses in time- and safety-critical applications.

At the end of the afternoon, all speakers will assemble in a panel format for an open discussion with the audience on the challenges in all aspects of automotive bus systems.

This all-day forum encourages an open information exchange in a closed environment. Attendance is limited, and pre-registration is required. Coffee breaks and a lunch break will be provided to allow participant to mingle and discuss issues of mutual interest.

Forum Agenda

Time	Topic
8:00	Breakfast
8:30	**Welcome and Introduction** **Wolfgang Pribyl,** *Graz University of Technology, Graz, Austria*
8:40	**Overview of Systems and Standards** **Herman Casier,** *AMI Semiconductor, Oudenaarde, Belgium*
9:10	**The New BMW X5 – Criteria for Bus System Selection and Optimization** **Martin Peteratzinger,** *BMW, Munich Germany*
10:00	**The Physical Layer of LIN and CAN-Bus, Driven by Cost and Automotive Requirements** **Geert Vandensande,** *AMI Semiconductor, Vilvoorde, Belgium*
10:50	Break
11:10	**Physical Layer of the Flexray Bus, Characteristics & Design Considerations** **Harald Gall,** *austriamicrosystems, Unterpremstaetten, Austria*
12:00	Lunch
1:30	**Protocols & Processors for Bus Systems, Example Flexray** **Shunichi Ko,** Fujitsu, Japan
2:20	**The MOST Network for the Multimedia Enabled Automobile** **Dave Knapp,** *SMSC, Austin, TX*
3:10	Break
3:30	**Safety and Dependability – a System Perspective** **Stefan Poledna,** *TTTech & Vienna University of Technology, Austria*
4:20	Panel Discussion
5:00	Conclusion

F6: Adaptive Techniques for Dynamic Processor Optimization

Organizer/Chair: **Shannon Morton**, *Icera Inc., Bristol, UK*

Committee:
Alice Wang, *Texas Instruments, Dallas, TX*
Bill Bowhill, *Intel, Hudson, MA*
Georgios Konstadinidis, *Sun Microsystems, Sunnyvale, CA*
James Warnock, *IBM, Yorktown Heights, NY*
Jos Huisken, *Silicon Hive, Eindhoven, Netherlands*
Hiroshi Makino, *Renesas, Hyogo, Japan*
Samuel Naffziger, *AMD, Fort Collins, CO*
Peter Kogge, *University of Notre Dame, Notre Dame, IN*
Norman Rohrer, *IBM, Essex Junction, VT*

One of the most severe repercussions of device scaling in sub-100nm technologies is the large variability in device parameters. This results in a wide range of operating points for manufactured silicon. Furthermore, there is a need to limit power and thermal dissipation to meet overall system or reliability concerns whilst still achieving sufficient performance for each software/system application. As a result, numerous innovative techniques have been developed to allow silicon-based functions to adjust dynamically to achieve their target operating point. Implementing such techniques spans the entire spectrum of design from devices and circuits through to testability and software/system control mechanisms.

In their presentations, the experts assembled for this forum will detail the various issues encountered in designing and utilizing dynamically adaptive systems. This forum is intended for chip designers at all levels who are interested in understanding the opportunity presented by dynamically adaptive chips and systems and the techniques to implement them.

The first talk by **David Scott** (TI), "Technology Challenges of Adaptive Techniques", will set the stage for the forum by explaining the technology scaling issues that have contributed to an ever widening range of post-fabrication behavior. **Koichiro Ishibashi** (Renesas) will then present "Adaptive Body Bias Techniques for Low Power SOC". This talk will focus on various methods of static and dynamic body biasing primarily applied to low power designs.

The next two talks discuss dynamically adaptive techniques for high end microprocessor-based systems. "Adaptive Control for High End Processor Power Management" by **Thomas Pflüger** (IBM) will address the voltage vs. frequency control mechanisms as well as various fundamental architectural techniques to dynamically manage power. **Mike Clark** (AMD) will follow with "Processor Support for Advanced Power and Thermal Management Techniques in Multi-core Environments". This talk will address issues such as detailed thermal monitoring, clock domains, and the software control loop, all in the context of a multi-core environment.

The fifth presentation by **David Blaauw** (U Michigan), "Adaptive Architectural Techniques and the Hardware/Software Interface", comes in two parts. The first will review some of the most useful architectural techniques that can be employed to manage power vs. performance on a dynamic basis. The second part will address a specific method known as "Razor" which dynamically corrects for timing-based errors on chip. Finally, **Eric Fetzer** (Intel) will discuss the challenges in testing, debugging, and practically implementing dynamically adaptive systems in his talk "The Challenges of Testing Adaptive Techniques".

Join us for a full day of expert analysis and presentation.

The all-day forum encourages open interchange and discussion. Attendance is limited and pre-registration is required. Breakfast, lunch, and coffee breaks will be provided to allow for a chance for participants to mingle and discuss the issues.

Forum Agenda

Time	Topic
	Breakfast
8:45	**Welcome and Overview** **Shannon Morton,** *Icera Inc., Bristol, UK*
9:00	**Technology Challenge of Adaptive Techniques** **David Scott,** *Texas Instruments, Dallas, TX*
10:00	**Adaptive Body Bias Techniques for Low Power SOC** **Koichiro Ishibashi,** *Renesas, Tokyo, Japan*
11:00	Coffee Break
11:15	**Adaptive Control for High End Processor Power Management** **Thomas Pflüger,** *IBM, Boeblingen, Germany*
12:15	Lunch
1:15	**Processor Support for Advanced Power and Thermal Management Techniques in Multi-core Environments** **Mike Clark,** *AMD, Austin, TX*
2:15	**Adaptive Architectural Techniques and the Hardware/Software Interface** **Dave Blaauw,** *University of Michigan, Ann Arbor, MI*
3:15	Coffee Break
3:30	**The Challenges of Testing Adaptive Techniques** **Eric Fetzer,** *Intel, Fort Collins, CO*
4:30	Open Panel Discussion & Final Wrap-up

F7: Low-Voltage Analog Amplifier Design for Filtering and A/D Conversion

Organizer/Chair: **Peter Kinget**, *Columbia University, New York, NY*

Committee: **Andrea Baschirotto**, *University of Lecce, Lecce, Italy*
JoAnn Close, *Analog Devices, San Jose, CA*
Axel Thomsen, *Silicon Laboratories, Austin, TX*

Analog designers are forced to deal with continuously decreasing supply voltages. Continued process scaling is reducing device dimensions including the gate oxide thickness and, as a result, the breakdown voltage and maximum supply voltage decrease for each process generation. Additionally, the increased use of battery-powered devices motivates the push toward lower supply voltages in mobile applications. While threshold voltages are not significantly lower, the net usable voltage range for signal swing, biasing, and device stacking is substantially reduced. As a result, amplifier performance (e.g., speed, gain and noise) is compromised, which then requires adjustments in the systems where they are applied.

This forum addresses the basic design issues for low-voltage amplifier circuits in the context of the applications and systems they operate in. A panel of researchers from academia and industry will review low-voltage amplifier design techniques, amplifier performance degradation due to low-voltage operation, as well as filter and A/D converter architecture solutions to mitigate the amplifier design challenges. The presented techniques will range from product-proven established techniques to more recently developed techniques for aggressive supply voltage scaling.

Andrea Baschirotto (U Lecce) will discuss active RC filter design solutions that incorporate limited opamp gain and bandwidth in the filter design process. **Peter Kinget's** (Columbia U) talk addresses circuit-level techniques that allow amplifiers to operate at extremely low supplies in filters and converters by utilizing techniques such as bulk biasing or bulk inputs, common-mode level shifting and switch elimination techniques. **Un-Ku Moon** (Oregon State U) will cover low-voltage, switched-circuit techniques for switched-capacitor and filter applications. **Willy Sansen** (KU Leuven) will address the issue of noise optimization in headroom-constrained amplifiers. In low supply environments, high-gain amplifiers need to be implemented as multistage amplifiers and **Johan Huijsing** (TU Delft) will present class-AB techniques as well as compensation techniques that stabilize amplifiers with up to 4 stages. **Jieh-Tsorng Wu** (National Chiao-Tung U) addresses the performance limitations that amplifiers cause in A/D converters and digital calibration techniques to overcome the amplifier imperfections. The final two presentations focus on how the constraints of low-voltage amplifier design result in engineering decisions. Battery-powered hearing aid IC designs require both low-voltage and low power and **Alexander Heubi** (AMIS) will discuss a design using low-voltage circuits in some areas while choosing to boost the supply voltage in others. **Corey Petersen** (Analog Devices) will review the trade-offs in low-voltage design for performance driven applications and discuss under what conditions low-voltage design is really beneficial.

The forum will conclude with a panel discussion where the attendees have the opportunity to ask questions and share their views.

Forum Agenda

Time	Topic
8:00	Continental Breakfast
8:30	**Welcome and Introduction** **Peter Kinget**, *Columbia University, New York, NY*
8:40	**Critical Opamp Design Aspects for Low-Voltage Active RC Filters** **Andrea Baschirotto**, *University of Lecce, Lecce, Italy*
9:20	**True Low-Voltage OTAs for 0.5V Active Filters, THAs and CT $\Delta\Sigma$ Converters** **Peter Kinget**, *Columbia University, New York, NY*
10:00	**Switched-R applications of Low-Voltage Amplifiers** **Un-Ku Moon**, *Oregon State University, Corvallis, OR*
10:40	Break
11:00	**Low-noise Optimization for Low-Voltage Amplifiers** **Willy Sansen**, *Katholieke Universiteit Leuven, Leuven, Belgium*
11:40	**Low Voltage Multi-Stage Amplifiers** **Johan Huijsing**, *Technische Universiteit Delft, The Netherlands*
12:20	Lunch
01:40	**Calibration techniques for Low-Voltage Amplifier Non-Idealities in Pipelined ADCs** **Jieh-Tsorng Wu**, *National Chiao-Tung University, Taiwan*
02:20	**Low-Voltage Analog Front End for Digital Hearing Aids** **Alexander Heubi**, *AMIS, Switzerland*
03:00	**Performance Motivated Low-Voltage Analog Circuit Design** **Corey Petersen**, *Analog Devices*
03:40	Break
04:00	Panel Discussion
05:00	Conclusion